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IN THE ABSTRACT

An FET device ~~comprises a semiconductor structure~~ with a source island [[,]] and a drain island ~~over~~ is formed on a horizontal surface of a substrate comprising an insulating material. A channel structure formed over the horizontal surface of the substrate, which connects between the drain and the source, ~~with the channel structure~~ comprises ~~comprising~~ a ~~horizontal~~ planar semiconductor channel fin formed above a vertical fin, ~~with the~~ The planar ~~fin~~ and ~~the~~ vertical fins ~~having~~ form a T-shaped cross-section. The bottom of the vertical fin ~~is contact with~~ contacts the horizontal surface of the substrate and the planar fin ~~is in contact with~~ contacts the top of the vertical fin. A gate dielectric layer covers exposed surfaces of the channel structure. A gate electrode straddles the channel gate dielectric and the channel structure. ~~Then a~~ A sacrificial layer, e.g. ~~such as~~ $SiGe_2$ ~~is~~ deposited upon the substrate before forming the vertical fin, ~~which~~ may be ~~either~~ a semiconductor or dielectric material. The planar fin ~~is~~ comprises a semiconductor material such as Si, SiGe or Ge.